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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,175	06/23/2004	Han-Chang Kang	REAP0025USA	4174
27765	7590	08/26/2005		
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116				
			EXAMINER NGUYEN, LINH M	
			ART UNIT 2816	PAPER NUMBER

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

HA

Office Action Summary

Application No.

10/710,175

Applicant(s)

KANG ET AL.

Examiner

Linh M. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 June 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 June 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>7/21/05, 7/26/05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims 1-13 are presented in the instant application according to the Applicants' filing on 06/23/2004.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4-5, 7 and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Kameya (U.S. Patent No. 4,829,272).

With respect to claims 1 and 7, Kameya discloses, in Fig. 1, an apparatus and its corresponding method for generating a phase delay comprising a buffer [I] for buffering an input signal and outputting an output signal [3]; a DAC for outputting a control voltage [Vd] corresponding to a digital value representative of a phase delay, and a variable capacitor [Dv]

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coupled to the DAC and the buffer, the capacitance value of the variable capacitor corresponding to the control voltage, wherein by controlling the capacitance value, the apparatus adjusts the phase delay between the input signal and the output signal.

With respect to claims 4 and 11, Kameya discloses, in Fig. 1, that the variable capacitor is a voltage-controlled capacitor.

With respect to claims 5 and 12, Kameya discloses, in Fig. 1, that the voltage-controlled capacitor is a MOS-based voltage-controlled capacitor.

With respect to claim 10, Kameya discloses, in Fig. 1, that the control voltage generating step is implemented by a DAC.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2-3 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kameya (U.S. Patent No. 4,829,272).

With respect to claims 2-3 and 8-9, Kameya discloses all of the claimed limitations as expressly recited in claims 1 and 7. Kameya does not explicitly disclose the input signal being a clock signal or a RF signal. However, such a selection of input signal depends largely upon the requirements of device chosen for a specific function which dictate the best suited input signal to yield the optimal result. Therefore, to select the correct input signal for the circuit such as Kameya's for the stated purpose would have been deemed obvious to an artisan skilled in the art.

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6. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kameya (U.S. Patent No. 4,829,272) in view of Park (U.S. Patent No. 6,219,397).

With respect to claims 6 and 13, Kameya discloses all of the claimed limitations as expressly recited in claims 1 and 7 except for the voltage-controlled capacitor is a P+/N well junction voltage-controlled capacitor.

Park discloses, in column 6, lines 59-60, a p+/n-well junction voltage controllable capacitor.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure an apparatus for phase delaying with a P+/N well junction voltage-controlled capacitor as taught by Park in order to achieve a large tuning range since such circuit arrangement with the P+/N well junction voltage-controlled capacitor for the stated purpose has been a well known practice as evidenced by the teachings of Park (*see Park, col. 6, lines 59-60*).

Citation of Relevant Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Miller (U.S. Patent No. 6,816,031) discloses an adjustable delay transmission line.

Prior art Higuchi et al. (U.S. Patent No. 6,637,008) discloses, in Fig. 38, a data transmission circuit with variable capacitance elements and a DAC.

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Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**LINH MY NGUYEN
PRIMARY EXAMINER**